

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN	202	15

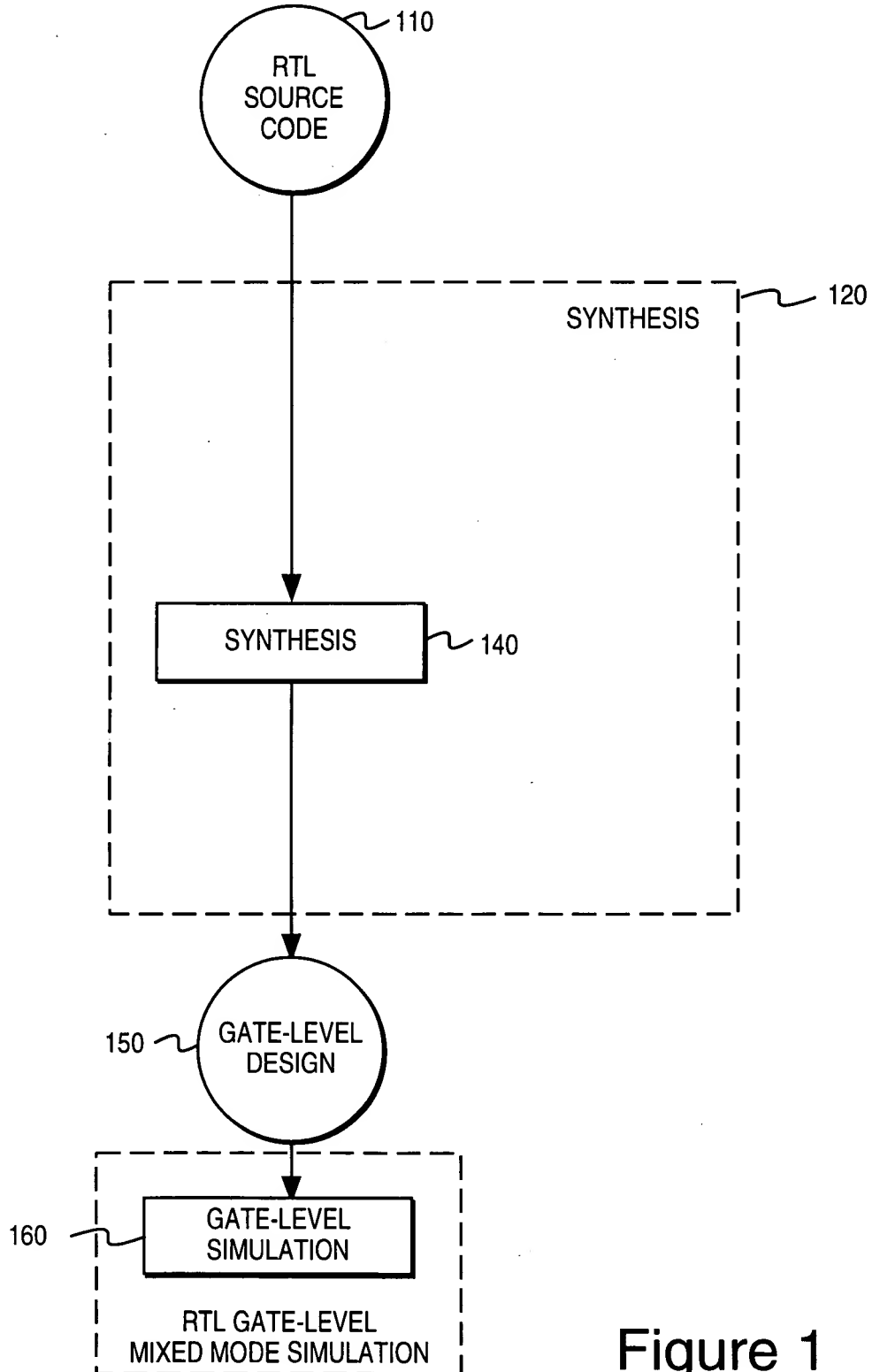


Figure 1

09127584-073198

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN	703	15

09127534-073193

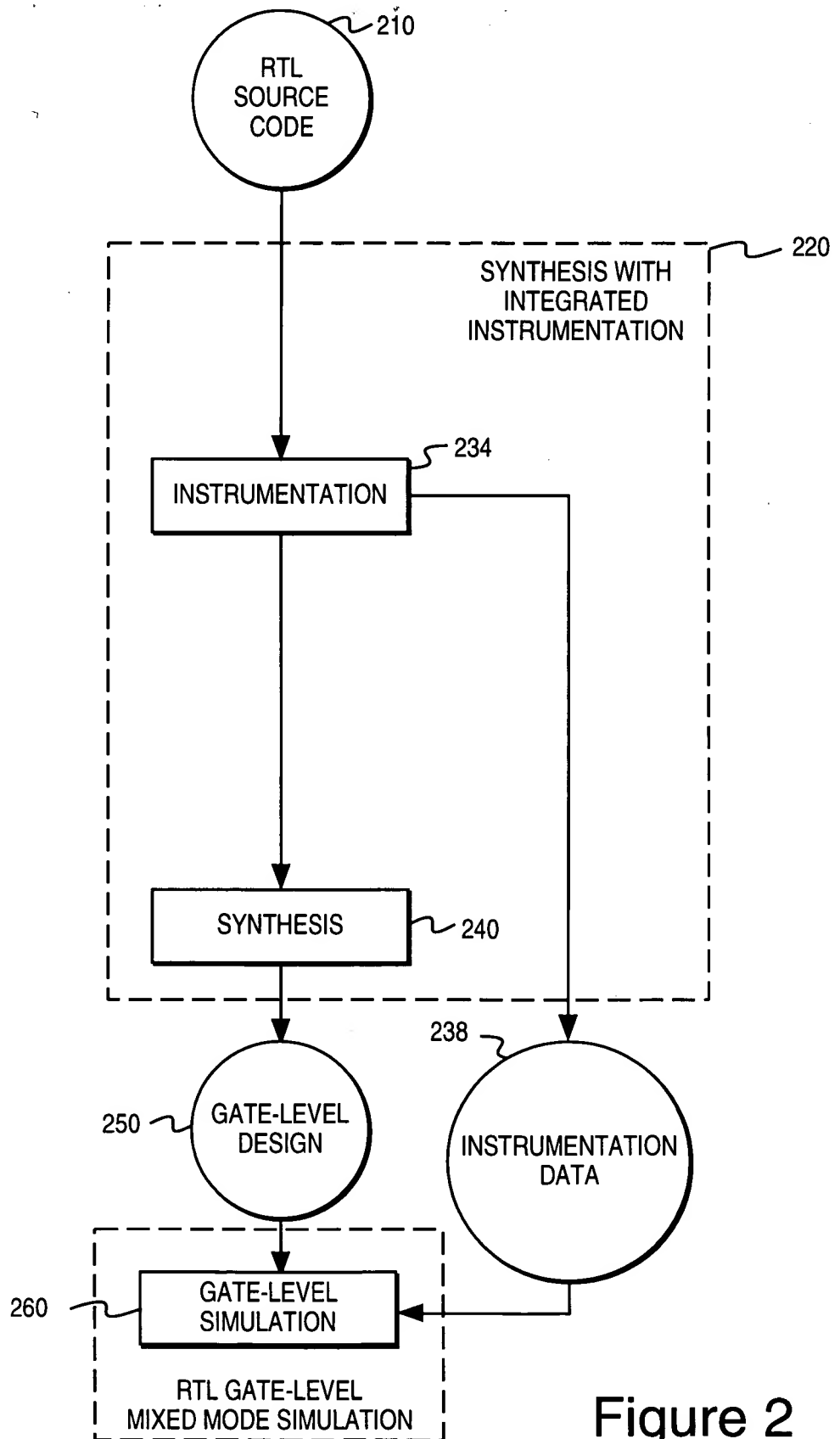


Figure 2

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

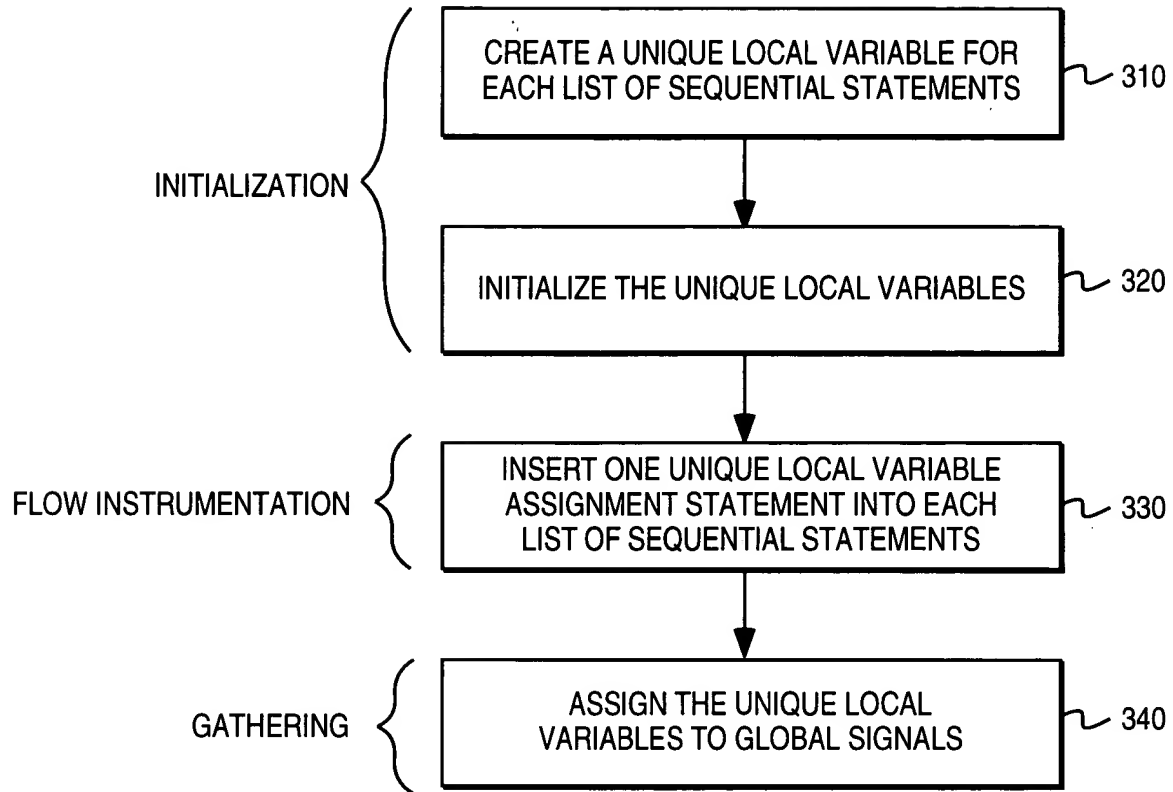


Figure 3

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APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

400

ENTITY ALOOP IS

PORT(  
 A : IN BIT\_VECTOR(0 TO 1);  
 RESET : IN BOOLEAN;  
 STATUS : OUT BOOLEAN);

END ENTITY ALOOP;

ARCHITECTURE RTL OF ALOOP IS

BEGIN

PROCESS(A, RESET)

VARIABLE ZEROS, ONES : INTEGER;

```

BEGIN
410 → IF(RESET)                                -- STATEMENT #1
      THEN
420 →   STATUS <= 0;                            -- STATEMENT #2
      ELSE
430 →   ZEROS := 0;                            -- STATEMENT #3
440 →   ONES := 0;                             -- STATEMENT #4
450 →   FOR I IN 0 TO 1 LOOP                   -- STATEMENT #5
460 →     IF A(I) = '0'                        -- STATEMENT #6
470 →     THEN                                -- STATEMENT #7
              ZEROS := ZEROS + 1;
480 →     ELSE                                -- STATEMENT #8
              ONES := ONES + 1;
              END IF;
      END LOOP;
490 →   STATUS <= (ZEROS > ONES);              -- STATEMENT #9
      END IF;

END PROCESS;

END ARCHITECTURE;
```

Figure 4

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

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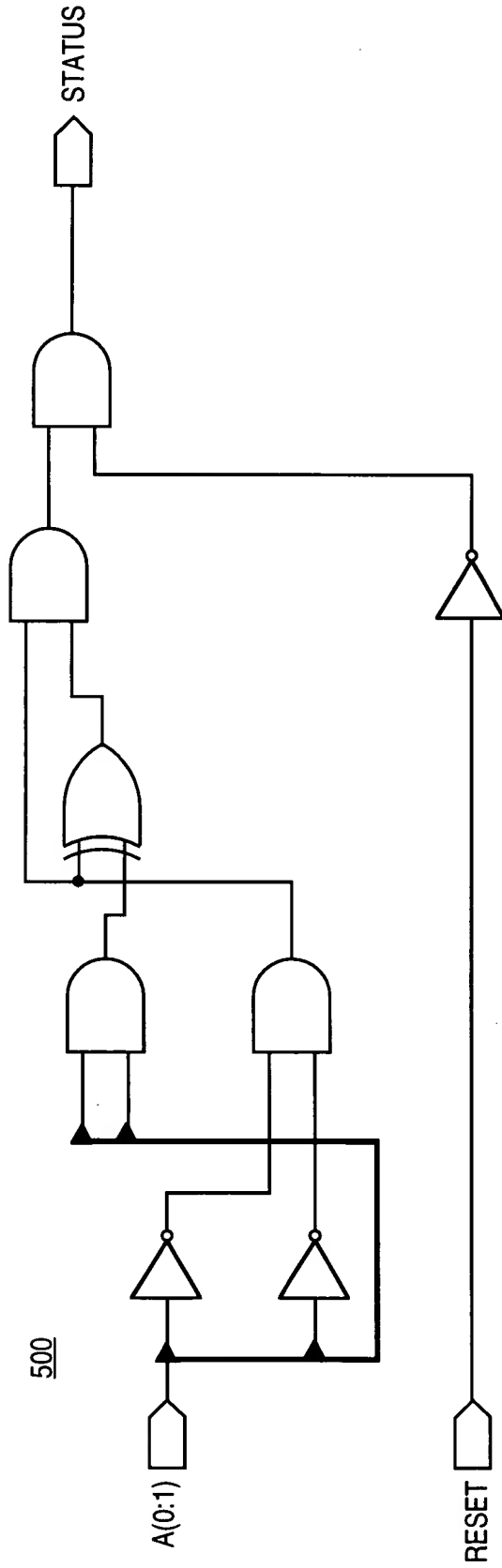


Figure 5

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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600

```

ENTITY ALOOP IS
PORT(
  A : IN BIT_VECTOR(0 TO 1);
  RESET : IN BOOLEAN;
  STATUS : OUT BOOLEAN;
  SIG_TRACE1, SIG_TRACE2, SIG_TRACE3, SIG_TRACE4, SIG_TRACE5,
  SIG_TRACE6 : OUT BIT
);
END ENTITY ALOOP ;

```

```

ARCHITECTURE RTL OF ALOOP IS
BEGIN
PROCESS(A, RESET)
  VARIABLE TRACE1, TRACE2, TRACE3, TRACE4, TRACE5, TRACE6 : BIT ;
  VARIABLE ZEROS, ONES : INTEGER ;

```

```

BEGIN
  TRACE1 := '0' ; TRACE2 := '0' ;
  TRACE3 := '0' ; TRACE4 := '0' ;
  TRACE5 := '0' ; TRACE6 := '0' ;

```

```

630 → TRACE1 := '1' ;           -- INSTRUMENT STATEMENT #1
      IF(RESET)                 -- STATEMENT #1
      THEN
632 → TRACE2 := '1' ;           -- INSTRUMENT STATEMENT #2
      STATUS <= FALSE ;         -- STATEMENT #2
      ELSE
634 → TRACE3 := '1' ;           -- INSTRUMENT STATEMENTS #3, #4, #5, #9
      ZEROS := 0 ;              -- STATEMENT #3
      ONES := 0 ;               -- STATEMENT #4
      FOR I IN 0 TO 1 LOOP      -- STATEMENT #5
636 → TRACE4 := '1' ;           -- INSTRUMENT STATEMENT #6
      IF A(I) = '0'             -- STATEMENT #6
      THEN
638 → TRACE5 := '1' ;           -- INSTRUMENT STATEMENT #7
      ZEROS := ZEROS + 1 ;      -- STATEMENT #7
      ELSE
640 → TRACE6 := '1' ;           -- INSTRUMENT STATEMENT #8
      ONES := ONES + 1 ;        -- STATEMENT #8
      END IF ;
      END LOOP ;
642 → STATUS <= (ZEROS > ONES) ; -- STATEMENT #9

```

```

END IF ;
SIG_TRACE1 <= TRACE1 ; SIG_TRACE2 <= TRACE2 ;
SIG_TRACE3 <= TRACE3 ; SIG_TRACE4 <= TRACE4 ;
SIG_TRACE5 <= TRACE5 ; SIG_TRACE6 <= TRACE6 ;
END PROCESS ;

```

```

END ARCHITECTURE ;

```

Figure 6

09127584-073198



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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800    MODULE SAMPLE(RESET, D, CLK, Q);

INPUT RESET ;  
INPUT D ;  
INPUT CLK ;  
REG Q ;  
OUTPUT Q ;

ALWAYS @(CLK OR RESET OR D)  
BEGIN

    IF(RESET==1)

        Q <= 0 ;

    ELSE

        IF(CLK==1)

            Q <= D ;

END

ENDMODULE

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0912/24-073108

Figure 8



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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MODULE SAMPLE(RESET, D, CLK, Q, SIG\_TRACE1, SIG\_TRACE2, SIG\_TRACE3, SIG\_TRACE4);

INPUT RESET;

INPUT D;

INPUT CLK;

REG Q;

900

OUTPUT Q;

REG SIG\_TRACE1, SIG\_TRACE2, SIG\_TRACE3, SIG\_TRACE4;

OUTPUT SIG\_TRACE1, SIG\_TRACE2, SIG\_TRACE3, SIG\_TRACE4;

INTEGER TRACE1, TRACE2, TRACE3, TRACE4;

ALWAYS @(CLK OR RESET OR D)

BEGIN

TRACE1 = 0; TRACE2 = 0; TRACE3 = 0; TRACE4 = 0;

TRACE1 = 1;

IF(RESET==1)

BEGIN

TRACE2 = 1;

Q <= 0;

END

ELSE

BEGIN

TRACE3 = 1;

IF(CLK==1)

BEGIN

TRACE4 = 1;

Q <= D;

END

END

SIG\_TRACE1 = TRACE1;

SIG\_TRACE2 = TRACE2;

SIG\_TRACE3 = TRACE3;

SIG\_TRACE4 = TRACE4;

END

ENDMODULE

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Figure 9

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

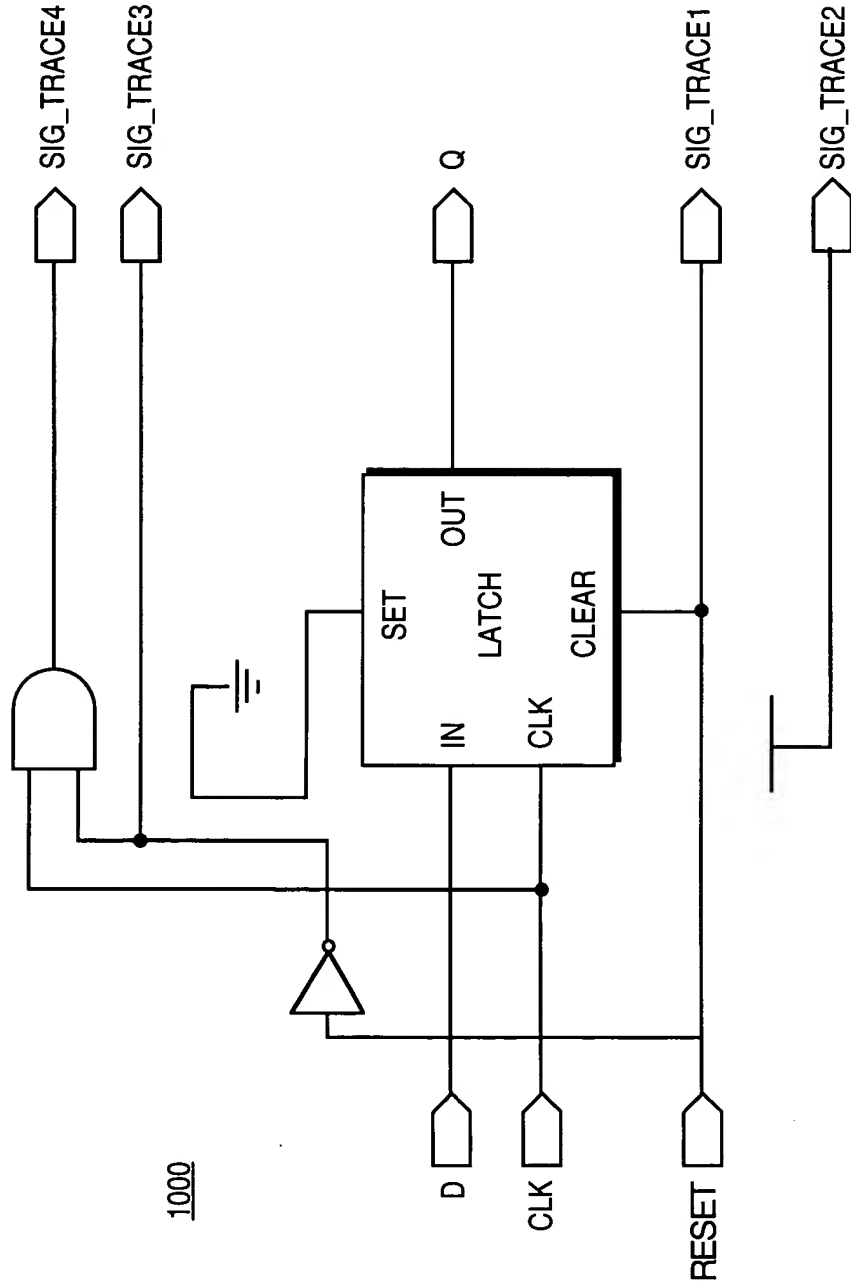


Figure 10

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

```

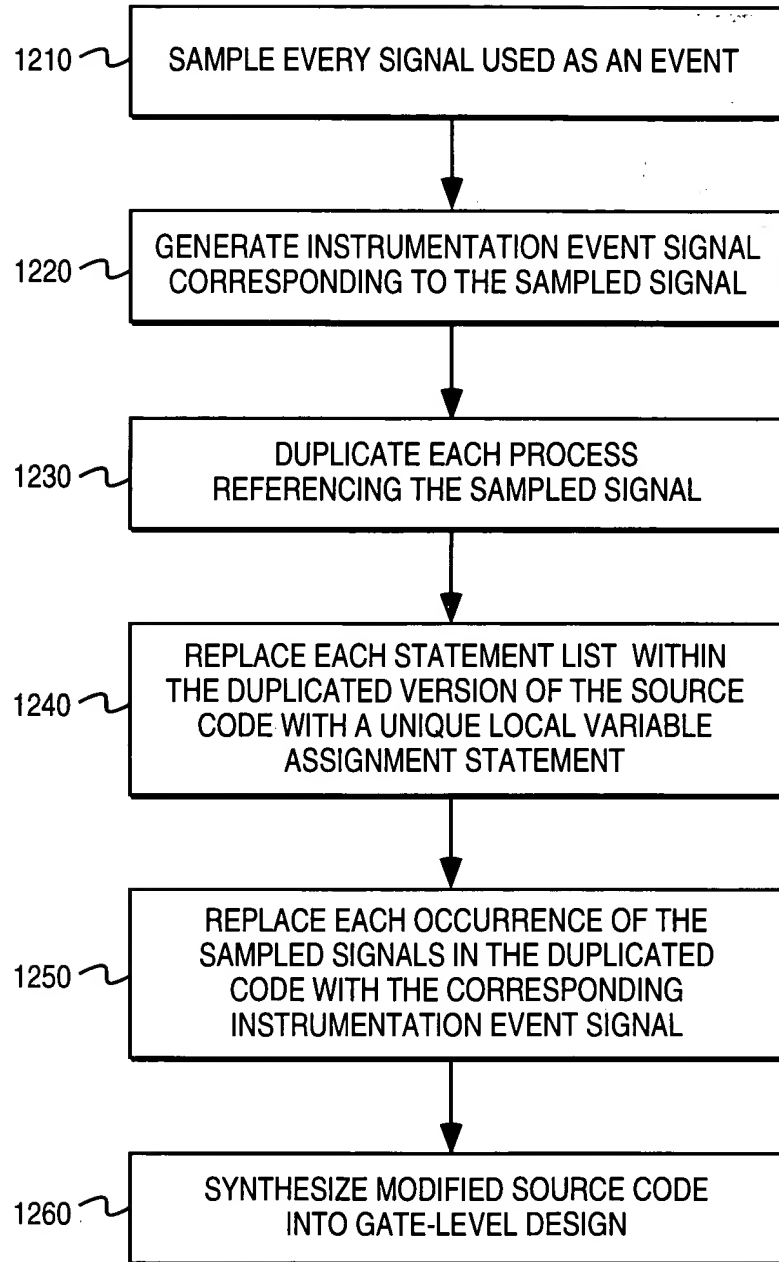
1100  PROCESS (CLK, D, RESET)
        BEGIN
            IF (RESET = '1') THEN
                Q <= '0';
            ELSIF (CLK'EVENT AND CLK = '1') THEN*
                Q <= D;
            END IF;
        END PROCESS

```

Figure 11

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APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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Figure 12

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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1300

```

PROCESS (FAST_CLK)
BEGIN
    IF (FAST_CLK'EVENT AND FAST_CLK = '1')
    THEN
        SAMPLED_CLK <= CLK;
    END IF
END PROCESS;

```

1310

```

CLK_EVENT <= SAMPLED_CLK /= CLK;
CLK_STABLE <= SAMPLED_CLK = CLK;
CLK_LASTVALUE <= SAMPLED_CLK;

```

```

PROCESS (CLK, D, RESET, CLK_EVENT)
    VARIABLE TRACE1, TRACE2 : BIT;
BEGIN
    TRACE1 := '0'; TRACE2 := '0';
    IF (RESET = '1') THEN
        TRACE1 := '1';
        Q <= '0';
    ELSIF (CLK_EVENT AND CLK = '1') THEN
        TRACE2 := '1';
        Q <= D;
    END IF;
    SIG_TRACE1 <= TRACE1; SIG_TRACE2 <= TRACE2;
END PROCESS;

```

1320

```

PROCESS (CLK, D, RESET)
BEGIN
    IF (RESET = '1') THEN
        Q <= '0';
    ELSIF (CLK'EVENT AND CLK = '1') THEN
        Q <= D;
    END IF;
END PROCESS

```

1330

Figure 13

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APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

1400

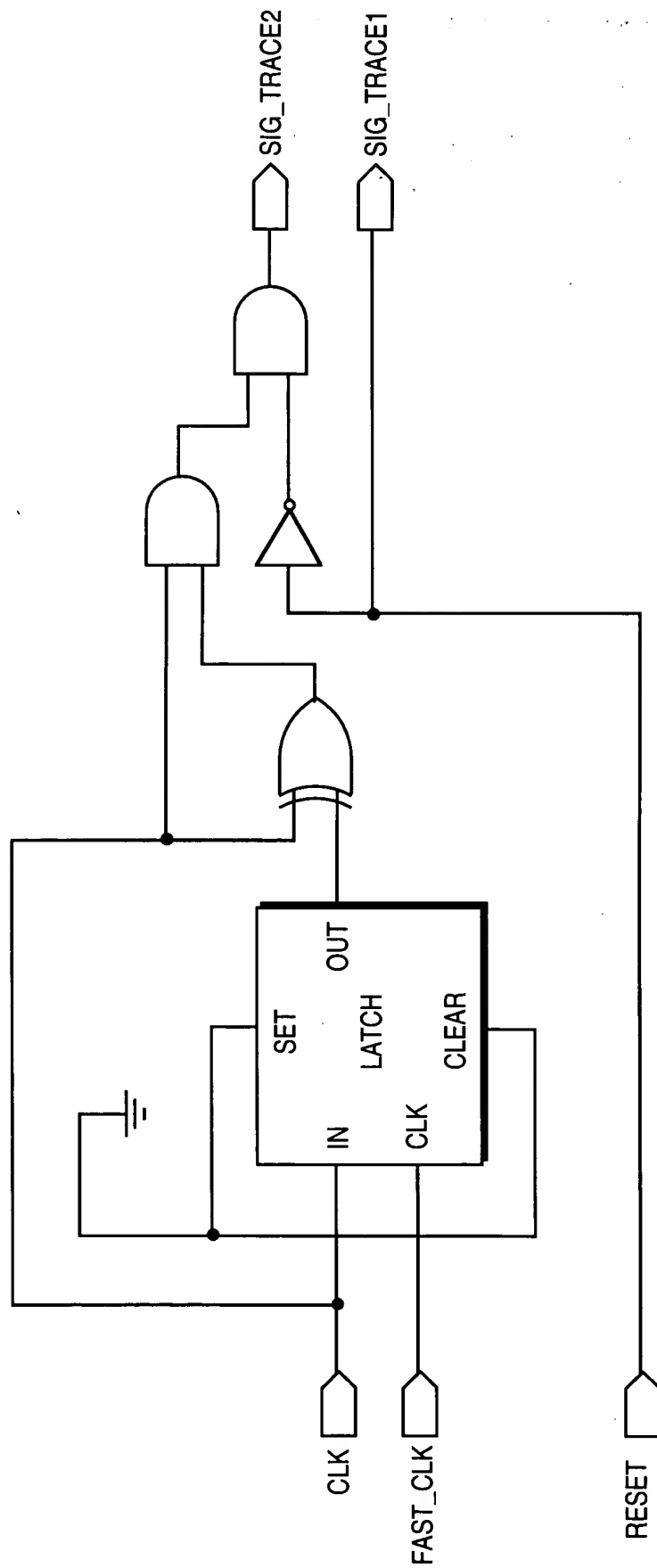


Figure 14

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

```

1500  ALWAYS @(POSEDGE CLK OR NEGEDGE RESET)
      BEGIN
          IF (RESET == 0)
              Q <= 0;
          ELSE
              Q <= D;
      END

```

## Figure 15

```

1600  ALWAYS @(POSEDGE FAST_CLK)
      BEGIN
          SAMPLED_CLK <= CLK
          SAMPLED_RESET <= RESET;
      END

      ASSIGN CLK_EDGE = SAMPLED_CLK ^ CLK;
      ASSIGN RESET_EDGE = SAMPLED_RESET ^ RESET;

      INTEGER TRACE1, TRACE2;
      REG [1:0] SIG_TRACE;
      ALWAYS @(CLK_EDGE OR RESET_EDGE OR CLK OR RESET)
      BEGIN
          TRACE1 = 0; TRACE2 = 0;
          IF((CLK_EDGE == 1) && (CLK == 1) && (RESET_EDGE == 1) && (RESET == 0))
              IF (RESET == 0)
                  TRACE1 = 1;
              ELSE
                  TRACE2 = 1;
              SIG_TRACE[0] = TRACE1;
              SIG_TRACE[1] = TRACE2;
          END

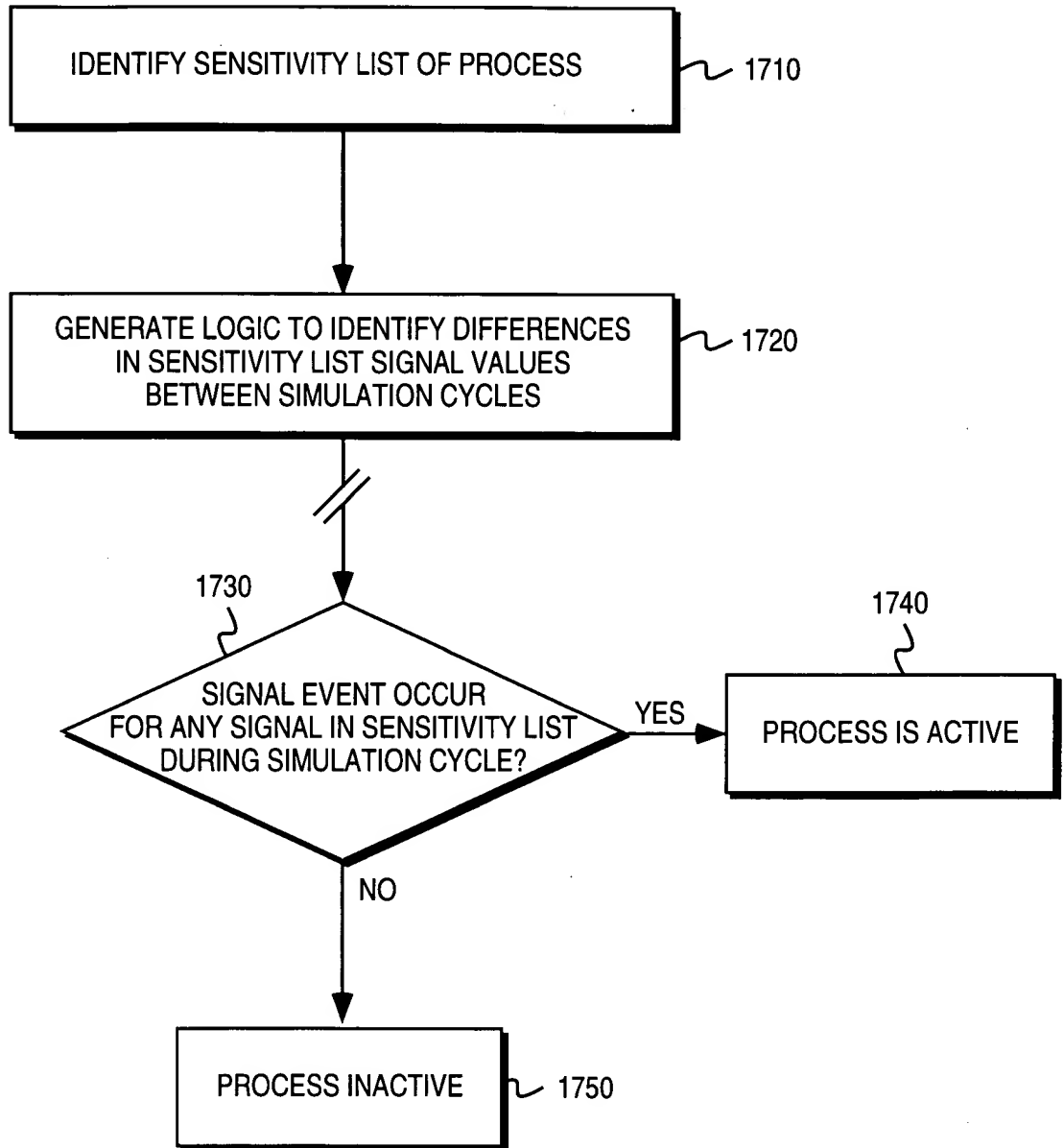
      ALWAYS @(POSEDGE CLK OR NEGEDGE RESET)
      BEGIN
          IF (RESET == 0)
              Q <= 0;
          ELSE
              Q <= D;
      END

```

## Figure 16

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APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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09127584-073198

Figure 17



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

P1: PROCESS (A, B, C)

```

PROCESS (FAST_CLK)
BEGIN
    IF (FAST_CLK'EVENT AND FAST_CLK = '1')
    THEN
        SAMPLED_A <= A;
        SAMPLED_B <= B;
        SAMPLED_C <= C;
    END IF
END PROCESS;

```

1810

```

P1_ACTIVE <= (SAMPLED_A /= A)
            OR (SAMPLED_B /= B)
            OR (SAMPLED_C /= C);

```

1820

Figure 18

09127534-073198

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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1910 CASE OPCODE IS  
 WHEN "00" => TRACE1 := 1;  
 STATE := 1;  
 WHEN "01" => TRACE2 := 1;  
 STATE := 2;  
 WHEN "10" => TRACE3 := 1;  
 STATE := 2;  
 WHEN "11" => TRACE4 := 1;  
 STATE := 1;  
 END CASE;

Figure 19

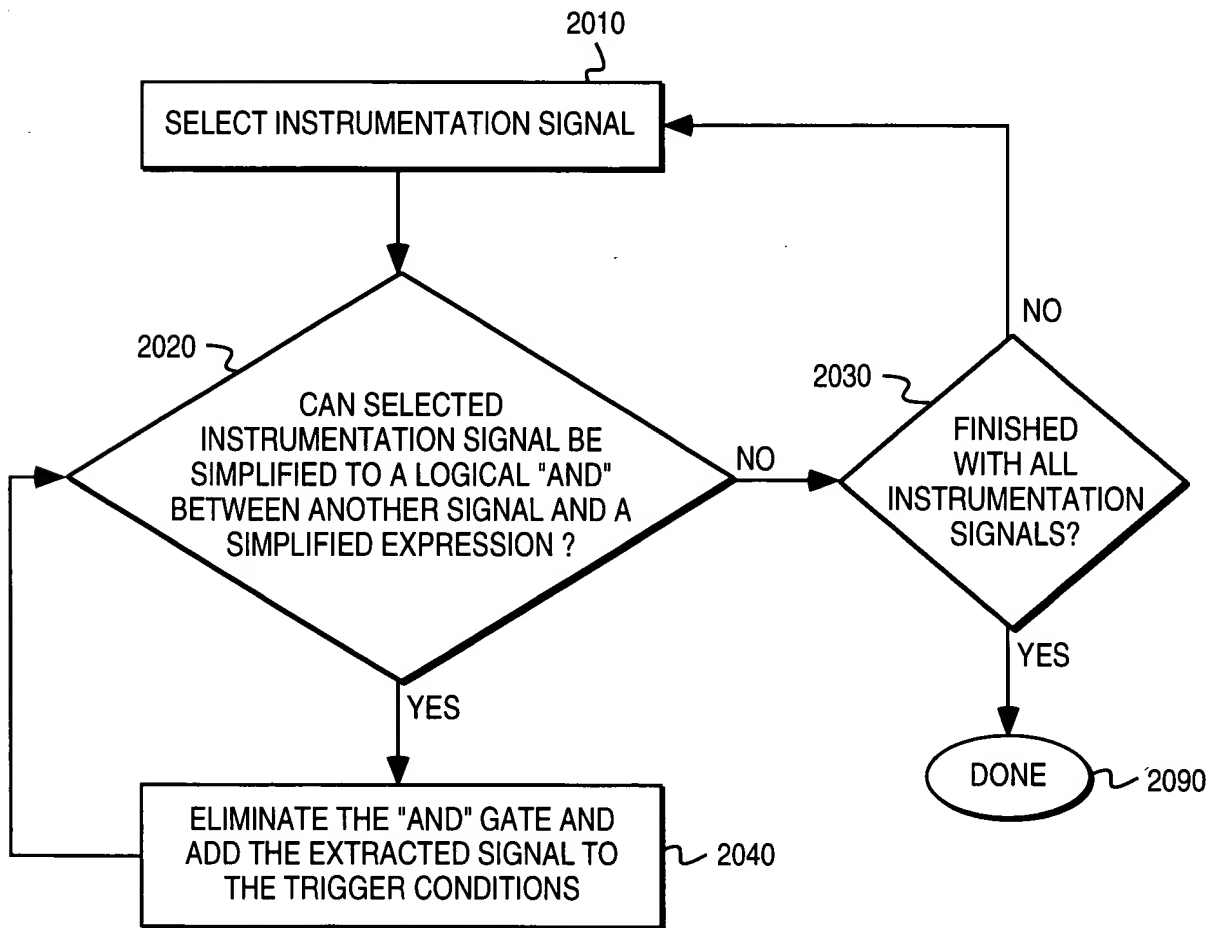


Figure 20

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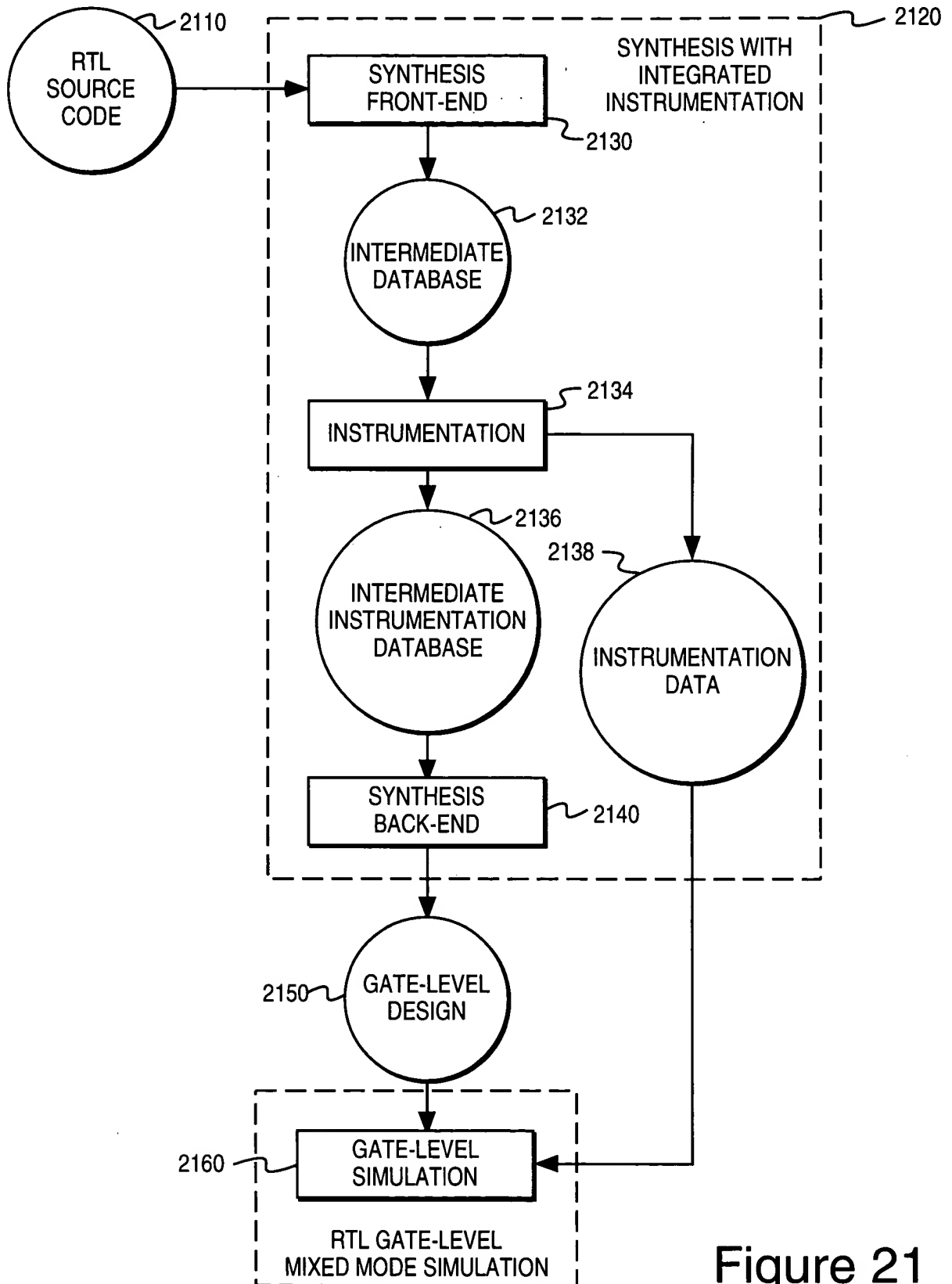


Figure 21

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APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

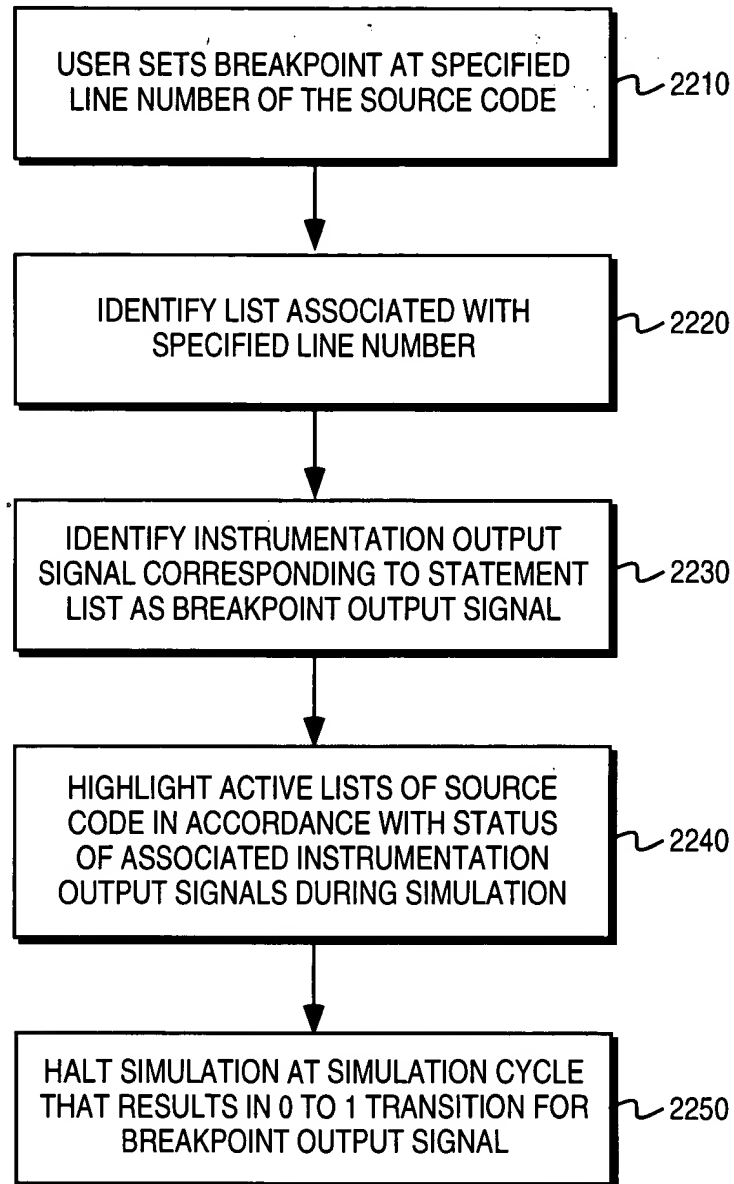


Figure 22

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